REMARKS

In the Non Final Office Action of January 22, 2007, the Examiner (1) rejected claims 1-7, 12-16 and 18-27 as allegedly unpatentable under 35 U.S.C § 112 1st paragraph (2) rejected claims 8-11 as allegedly anticipated by Feierbach et al. (U.S. Patent No. 6,088,786); (3) rejected claims 1-2, 4, and 6-7 as allegedly obvious over Feierbach and Batten et al. (U.S. Patent No. 6,256,725); (4) rejected claim 3 as allegedly obvious over Feierbach, Batten and Patel (U.S. Patent No. 6,826,749) and (5) rejected claim 5 as allegedly obvious over Feierbach, Batten and Gee et al. (U.S. Patent No. 6,374,286); (6) rejected claims 12-15, 18-24, and 27 as allegedly obvious over Feierbach, Patel, Batten and Hennessy et al. ("Computer Architecture: A Quantitative Approach."); (7) rejected claims 16 and 26 as allegedly obvious over Feierbach, Patel, Batten, Hennessy and Gee; (8) rejected claim 25 as allegedly obvious over Feierbach, Patel, Batten, Hennessy, Hendler et al. (U.S. Patent No. 6,473,777) and Brassac et al. (U.S. Patent No. 6,928,539); (9) rejected claims 30-35, 37 and 41 as allegedly obvious over Feierbach and Hendler; (10) rejected claim 36 as allegedly obvious over Feierbach, Hendler and Patel; and (11) rejected claims 38-40 as allegedly obvious over Feierbach, Hendler and Gee.

Based on the arguments contained herein, Applicants respectfully request reconsideration and allowance.

I. 35 U.S.C. § 112 1st PARAGRAPH BASED REJECTION

Claims 1-7, 12-16 and 18-27 stand rejected allegedly for failing to comply with written description requirement.

In office action claim 1 and 12 stands rejected for failing to comply with the written description requirement. In particular, the Office Action states that the limitation "wherein said logic executes instructions from both said stack-based instruction set and said second instruction set" has no support in the specification as filed. To address these concerns, Applicants direct the Examiner to at least Figure 2, the JSM 102, as well as corresponding paragraph [0024] of the specification. In the disclosed embodiment, the JSM 102 is adapted to process and execute instructions from at least two instruction sets. One instruction set includes stack-based operations and the second instruction set includes register-based and memory-based operations. Hence, the JSM can execute both instruction sets.

Based on the foregoing, Applicants respectfully requests that the 35 USC § 112 1st paragraph written description requirement rejection be withdrawn.

II. ART BASED REJECTIONS

A. Claim 1

Claim 1 stands rejected as allegedly obvious over Feierbach and Batten.

Feierbach is directed towards coupling a stack based processor to a register based functional unit. (Feierbach Title). In particular, Feierbach teaches a stack processor and register processor as part of a stack and register processor. (Feierbach Col. 6, lines 53-59). Further, Feierbach discloses a copy-unit to control access of data between the processors. (Feierbach Abstract). Moreover, Feierbach teaches that the processor fetches stack instructions, and decodes the fetched stack instructions to determine if they are regular stack instructions or extended stack instructions. (Feierbach Col. 5, lines 62-67 to Col. 7, lines 1-7). Therefore, it appears that Feierbach teaches fetching and executing only one set of instructions (i.e. stack-based instructions). Further, the Examiner concedes that "Feierbach failed to teach wherein said logic executes instructions from both said stack-based and said second instruction set." (Office Action Page 7).

Batten is directed towards a shared datapath processor utilizing stack-based and register-based storage spaces. (Batten Title). In particular, Batten discloses a datapath which can be selectively coupled to each of the architecturally distinct storage spaces, such that instructions for each of the spaces may be interspersed. (Batten Col. 3, lines 22-34)

Claim 1, by contrast, specifically recites "**a plurality of registers contained in said core and coupled to the logic and addressable through a second instruction set** that provides register-based and memory-based operations." Applicants submit that Feierbach and Batten fail to teach or fairly suggest such a processor. In particular, Feierbach teaches a processor that fetches and executes only one set of instructions (i.e. stack-based instructions). Further, the Examiner concedes that "Feierbach failed to teach wherein said logic executes instructions from both said stack-based and said second instruction set." Thus, even if the teachings of Batten are precisely as the Office Action suggests (which Apps do not admit), Feierbach and Batten still fail to teach or suggest a processor as required by claim 1. Specifically, the art of record does not teach or suggest a processor that comprises a core that has both registers and a stack, wherein the core executes both

a stack-based instruction set in conjunction with the stack and a second instruction set to address the registers.

Based on the foregoing Applicants submit that claim 1, and all claims which depend on claim 1 (claims 2-7), should be allowed.

B. Claim 8

Claim 8 stands rejected as allegedly anticipated by Feierbach.

Claim 8 specifically recites "fetch logic **receiving instructions from a second instruction set which comprises memory-based and register-based instructions**." Applicants submit that Feierbach fails to expressly or inherently teach such a method. In particular, Feierbach teaches a processor that fetches and executes only one set of instructions (i.e. stack-based instructions). Further, the Examiner concedes that "Feierbach failed to teach wherein said logic executes instructions from both said stack-based and said second instruction set." (Office Action Page 7). Thus, Feierbach still fails to expressly or inherently teach the method as required by claim 8. Specifically, the art of record does not teach or suggest a processor that comprises a core that has both registers and a stack, wherein the core executes both a stack-based instruction set in conjunction with the stack and a second instruction set to address the registers.

Based on the foregoing Applicants submit that claim 8, and all claims which depend on claim 8 (claims 9-11), should be allowed.

C. Claim 12

Claim 12 stands rejected as allegedly obvious over Feierbach, Patel, Batten and Hennessey.

Claim 12 specifically recites "a plurality of registers contained in said core and **coupled to the logic and addressable through a second instruction set that provides register-based and memory-based operations**." Applicants submit that Feierbach, Patel, Batten and Hennessey fail to teach or fairly suggest such a processor. In particular, Feierbach teaches a processor that fetches and executes only one set of instructions (i.e. stack-based instructions). Further, the Examiner concedes that "Feierbach failed to teach wherein said logic executes instructions from both said stack-based and said second instruction set." (Office Action Page 12). Thus, even if the teachings of Patel, Batten and Hennessy are precisely as the Office Action suggests (which Apps do not admit), Feierbach and Batten still fail to teach or suggest a processor as required by claim 12.

Specifically, the art of record does not teach or suggest a processor that comprises a core that has both registers and a stack, wherein the core executes both a stack-based instruction set in conjunction with the stack and a second instruction set to address the registers.

Based on the foregoing Applicants submit that claim 12, and all claims which depend claim 12, (claims 13-16 and 18-27), should be allowed.

D. Claim 30

Claim 30 stands rejected as allegedly obvious over Feierbach and Hendler.

Claim 30 specifically recites "the core of the co-processor is configured to execute the stack-based instructions and **instructions from a second instruction set that provides memory-based and register-based operations**." Applicants submit that Feierbach, and Hendler fail to teach or fairly suggest such a system. In particular, Feierbach teaches a processor that fetches and executes only one set of instructions (i.e. stack-based instructions). Further, the Examiner concedes that "Feierbach failed to teach wherein said logic executes instructions from both said stack-based and said second instruction set." (Office Action Page 7). Thus, even if the teachings of Hendler are precisely as the Office Action suggests (which Apps do not admit), Feierbach and Hendler still fail to teach or suggest a processor as required by claim 30. Specifically, the art of record does not teach or suggest a processor that comprises a core that has both registers and a stack, wherein the core executes both a stack-based instruction set in conjunction with the stack and a second instruction set to address the registers.

Based on the foregoing Applicants submit that claim 30, and all claims which depend on claim 30 (claims 31-41), should be allowed.

III. CONCLUSION

In course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. If the Examiner feels that a telephone conference would expedite the resolution of this case, he is respectfully requested to contact the undersigned. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to the Texas Instruments, Inc. Deposit Account No. 20-0668.

Respectfully submitted,

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